Notes for Akai DR8, DAC card (8 ch)

Akai PCB assembly L3026A5080, PC DA8

100R between DGND on P1 (60 way IDC), and DGND of filter IC, possibly to help with ground loop management.

Test HDL runs in an EPM7128 clocked at 24.576MHz, and synthesizes a test signal (1kHz and 2kHz, FS, 18 bit data). Generates XTI, BC, LRCK, and DATA. Connect to +in of DS34C86 input buffer.

TRS output connector manufactured by Hosiden, Japan (http://www.hosiden.com/)

Digital filter (IC4, 5, 6 & 7), main format select pin 4 = '1'. This selects input data format, alignment, etc.

Clock select rate (pin 3) 256Fs.

Bit Clock In (pin 2) feeds both input filters.

INF1N (pin 4) hi, DI/INF2N (IC3, IC4, pin 1) lo: Input format 'LR alt leading data'

Left Data on IW1N/DIL (pin 5), Right Data on IW2N/RIL (pin 10). These pins are joined, so L+R data appears on a single input pin.

P2 carries ±8V to 5V regulators for digital filters and DACs

P3 carries ±12V for output op-amps and mute relays. Mute relays are controlled by TR2 (2SC144), and associated power up reset generator, IC9 (M51953). IC9 is attached to a 10uF timing cap, implying a couple of seconds of power up reset time. Mute relays normally un-powered, adding

TR1 (2SC144) appears to control mute of the digital input filters.

SW1, SW2... controls output level (+4, -10dBu), presumably associated with IC15, IC22...

Measured:

Rail	Current
+9V, filter & DAC	+280 mA
-9V, filter & DAC	-200 mA
+12V output op-amps + relays	+200 mA
-12V output op-amps	-100 mA

Feed single ended clocks into +inputs of input buffer (DS34C86).

Input buffer may be loaded at location IC3 or IC2, presumably selecting where data is positioned on the 60 way connector, and maybe the only difference between the 2nd 8ch DAC card used in the DR16 units.

Mark Atherton, New Zealand, 18 nov 2012