Notes for Akai DR8, ADC card (8 ch)

Akai PCB assembly L3026A5030, PC ADJACK

AK5389 18 bit ADCs, ~107dB dynamic range.

Input signal conditioning is split from ADC at P5, 6, 7 & 8, with balanced audio carried over this connector.

Input gain switch, presumably +4/-10dBu range (same as DAC assembly).

Output data carried over 74HC375 quad transparent latch - always enabled, so used as a differential buffer.

+ve regulators may be damaged as DAC board so, worth powering up digital section and clocking ASAP.

Input processing power (±12V) carried via P3, which is in parallel with P4.

R5 in series with XTI, connects to IC13 (3)

SMODE (pin 12) is lo, ADC in slave mode.

CMODE (pin 11) is lo, dividers accept 256Fs ICLKD input.

FSYNC (pin 17) is hi, "data is clocked out directly after L/R transition"

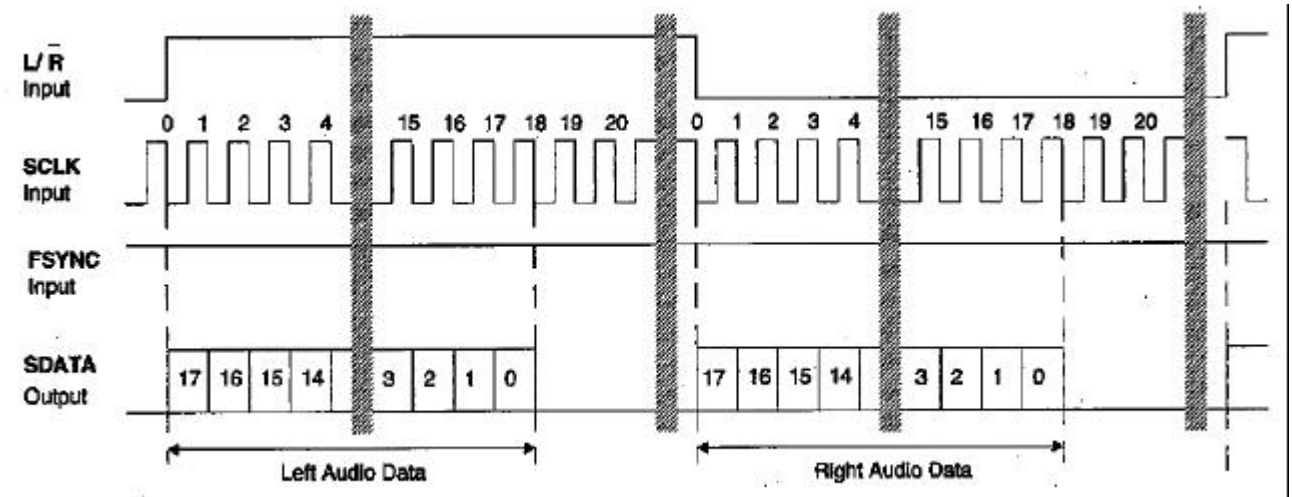

Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

Tie P1 (1), DPD+ [ADC8] low, to take ADC out of power down.

Ensure ±9V to ADC regs (on P2) is high enough to not cause power sense IC to re-trigger.

Each ADC analogue input touched with finger on probe, while monitoring associated converted data stream. All inputs appear to change bits in datastream.

Mark Atherton, New Zealand, 18 nov 2012

Rail	Current
+9V, ADC	+320 mA
-9V, ADC	-150 mA
+12V input op-amps	48 mA
-12V input op-amps	-48 mA

At ICLK = 12.288MHz